Amendments to Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (Currently Amended) A memory module, comprising:

a printed circuit board having opposing first and second outside surfaces;

a unibody via extending along an axis perpendicular to the first and second outside surfaces and extending entirely through the printed circuit board and coupled between a primary conductor on the first outside surface and a secondary conductor on the second outside surface;

at least one primary semiconductor memory device arranged upon the first outside surface and coupled to the primary conductor;

a memory controller coupled to the primary conductor; ~~and~~

at least one secondary semiconductor memory device arranged upon the second outside surface substantially opposite the primary semiconductor memory device and coupled to the secondary conductor; and

wherein the primary and secondary semiconductor memory devices each comprise a midpoint between outer lateral edges of each respective primary and secondary semiconductor memory device through which a single axis extends substantially perpendicular to the first and second outside surfaces.

2. (Canceled)

3. (Original) The memory module as recited in claim 1, wherein the primary and secondary semiconductor memory devices each comprise outer lateral edges that are directly opposite the printed circuit board from each other.

4. (Original) The memory module as recited in claim 1, wherein the at least one primary semiconductor memory device comprises a pair of primary semiconductor memory devices arranged on a first portion of the first outside surface, and wherein the at least one secondary semiconductor memory device comprises a pair of secondary semiconductor memory devices arranged on a second portion of the second outside surface substantially opposite the first portion.

5. (Previously Presented) The memory module as recited in claim 4, wherein a first one of the pair of primary semiconductor memory devices and a first one of the pair of secondary semiconductor memory devices comprise a first central point through which a first axis extends substantially perpendicular to the first and second outside surfaces; and wherein a second one of the pair of primary semiconductor memory devices and a second one of the pair of secondary semiconductor memory devices comprise a second central point through which a second axis extends a parallel, spaced distance from the first axis and substantially perpendicular to the first and second outside surfaces.

6. (Original) The memory module as recited in claim 1, wherein the printed circuit board further comprises:

a power supply conductor arranged upon a power supply plane dielectrically spaced between the first and second outside surfaces; and

a ground supply conductor arranged upon a ground supply plane dielectrically spaced between the first and second outside surfaces and also between the power supply plane and either the first outside surface or the second outside surface.

7. (Original) The memory module as recited in claim 1, wherein the printed circuit board consists of four conductive layers dielectrically separated from each other, and wherein two of the four conductive layers are on the first and second outside surfaces.

8. (Currently Amended) A memory module, comprising:

a printed circuit board consisting of four conductive layers dielectrically separated from each other, wherein a first pair of the four conductive layers are on opposed outside surfaces of the printed circuit board and a second pair of the four conductive layers are on dielectrically isolated, parallel inside surfaces of the printed circuit board;

a plurality of primary conductors arranged on one of the first pair of the four conductive layers;

a plurality of secondary conductors arranged on another one of the first pair of the four conductive layers;

a ground supply conductor arranged on one of the second pair of four conductive layers;

a power supply conductor arranged on another one of the second pair of four conductive layers;

a primary synchronous dynamic random access memory (SDRAM) packaged integrated circuit coupled to a power supply, and placed in a first slot on a first one of the opposed outside surfaces and coupled to a subset of the plurality of primary conductors;

a secondary synchronous dynamic random access memory (SDRAM) packaged integrated circuit coupled to the power supply, and placed in a second slot on a second one of the opposed outside surfaces and coupled to a subset of the plurality of secondary conductors; ~~and~~

wherein the first and second slots comprise bonding pads arranged on a portion of the respective first and second ones of the opposed outside surfaces to form a footprint in which the primary SDRAM is surface mounted substantially directly opposite the secondary SDRAM;

wherein the plurality of primary and secondary conductors are terminated at each respective end through pull-up resistors and output drivers connected to a reference supply; and

wherein the power supply conductor comprises at least two laterally spaced coplanar power supply conductors, and wherein one power supply conductor is coupled between the reference supply and the pull-up resistors and output drivers, and wherein the other power supply conductor is coupled between the power supply and the primary and secondary SDRAMs.

9. (Original) The memory module as recited in claim 8, wherein a midpoint between bonding pads which form the footprint on the first one of the opposed outside surfaces is linked by an axial line to the midpoint between bonding pads which form the footprint on the second one of the opposed outside surfaces, and wherein the axis line is perpendicular to the opposed outside surfaces.

10. (Canceled)

11. (Currently Amended) The memory module as recited in claim ~~10~~8, wherein the pull-up resistors and output drives comprise termination devices for connecting ends of the plurality of primary and secondary conductors according to stub series terminated logic (SSTL).

12. - 13. (Canceled)

14. (Original) The memory module as recited in claim 8, further comprising a memory controller placed on only one of the opposed outside surfaces and coupled directly to the plurality of primary conductors and coupled indirectly through vias extending through the printed circuit board to the plurality of secondary conductors.

15. (Original) The memory module as recited in claim 10, wherein the primary and secondary SDRAMs are packaged within a thin small outline package (TSOP) with leads extending from the TSOP solder bonded to corresponding bonding pads of the associated first and second slots.

16. (Original) The memory module as recited in claim 8 is a single in-line memory module (SIMM), a dual in-line memory module (DIMM), or is arranged on the same printed circuit board as an execution unit or processor.

17. (Currently Amended) A method for arranging memory devices upon a printed circuit board, comprising:

arranging a pair of packaged memory devices on opposing outside surfaces of the printed circuit board directly opposite one another with the midpoint of the pair arranged upon an axis that extends perpendicular to the opposing outside surfaces;

arranging a memory controller on a first one of the opposing outside surfaces;

in a single step, employing concurrent solder reflow:

surfacing mounting at least one lead extending from a first one of the pair of memory devices to a first end of a via extending perpendicularly through the printed circuit board and to a first end of a conductor extending across a first one of the opposing outside surfaces;

surface mounting at least one lead extending from the memory controller to a second opposed end of the conductor; ~~and~~

surface mounting at least one lead extending from a second one of the pair of memory devices to a second end of the via opposite the first end of the via; and

terminating the opposing first and second ends of the conductor with a pull-up resistor to a power supply having a voltage value dissimilar from a voltage value placed on the pair of packaged memory devices.

18. (Original) The method as recited in claim 17, further comprising extending the via through an aperture within a power supply planar element and a ground supply planar element dielectrically spaced from each other a dielectrically spaced distance between the opposing outside surface.

19. (Canceled)

20. (Original) The method as recited in claim 17, further comprising terminating the opposing first and second ends of the conductor according to stub series terminated logic (SSTL).